

BIAX Corporation v. Intel
Civil Action No. 2:05-cv-184-TJW

EXHIBIT 4
(PART 1)
FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

(12) **United States Patent**
Morrison et al.

(10) **Patent No.: US 6,253,313 B1**
(45) **Date of Patent: *Jun. 26, 2001**

(54) **PARALLEL PROCESSOR SYSTEM FOR PROCESSING NATURAL CONCURRENCIES AND METHOD THEREFOR**

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(73) Assignee: **Biax Corporation**, Palm Beach
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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

This patent is subject to a terminal dis-
claimer.

(21) Appl. No.: **08/480,691**

(22) Filed: **Jun. 7, 1995**

Related U.S. Application Data

(62) Division of application No. 08/254,687, filed on Jun. 6,
1994, now Pat. No. 5,517,628, which is a division of
application No. 08/093,794, filed on Jul. 19, 1993, now
abandoned, which is a continuation of application No.
07/913,736, filed on Jul. 14, 1992, now abandoned, which
is a continuation of application No. 07/560,093, filed on Jul.
30, 1990, now abandoned, which is a division of application
No. 07/372,247, filed on Jun. 26, 1989, now Pat. No.
5,021,945, which is a division of application No. 06/794,
221, filed on Oct. 31, 1985, now Pat. No. 4,847,755.

(51) Int. Cl.⁷ **G06F 13/00**

(52) U.S. Cl. **712/226; 712/228; 712/233;**
712/234

(58) Field of Search **712/1, 11, 226,**
712/228, 233, 234

(56) **References Cited**

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Primary Examiner—Meng-Al T. An

(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(57) **ABSTRACT**

A computer processing system containing a plurality of identical processor elements each of which does not retain execution state information from prior operations. The plurality of identical processor elements operate on a statically compiled program which, based upon detected natural concurrencys in the basic blocks of the programs, provide logical processor numbers and an instruction firing time to each instruction in each basic block. Each processor element is capable of executing instructions on a per instruction basis such that dependent instructions can execute on the same or different processor elements. A given processor element is capable of executing an instruction from one context followed by an instruction from another context through use of shared storage resources.

25 Claims, 17 Drawing Sheets

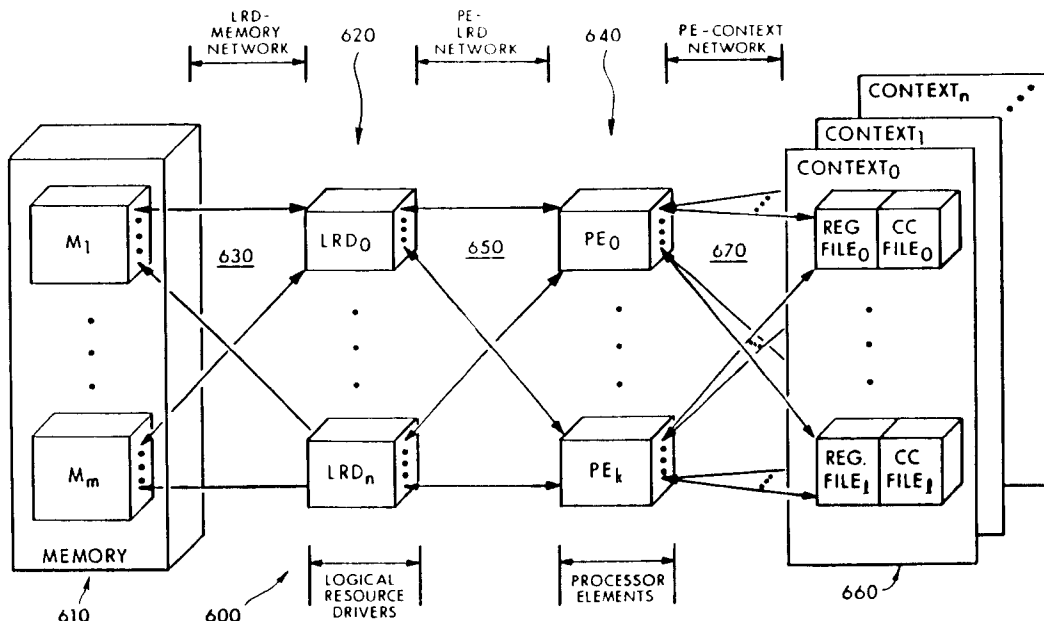


FIG. 1

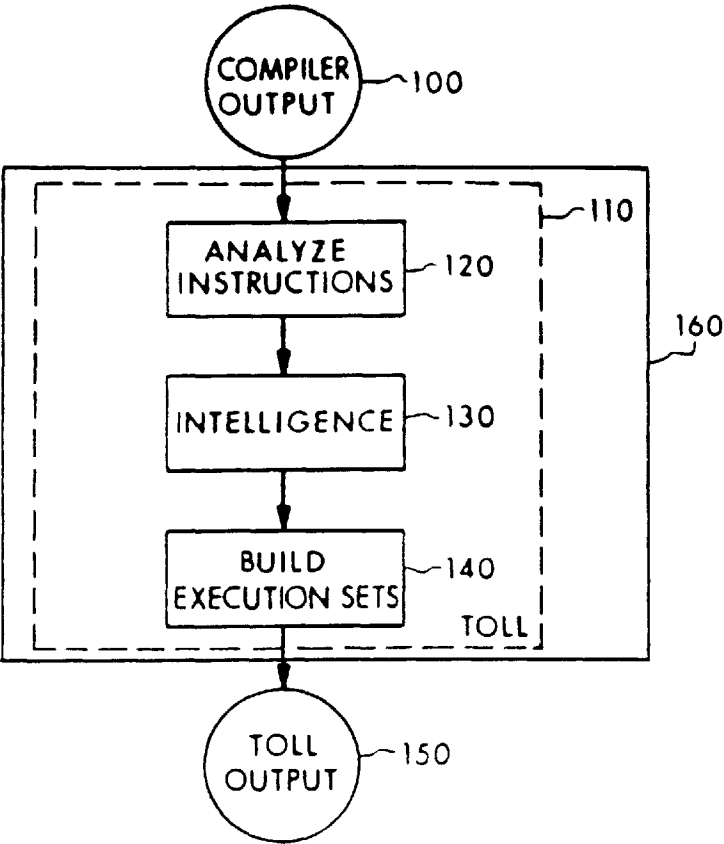


FIG. 2
PRIOR ART

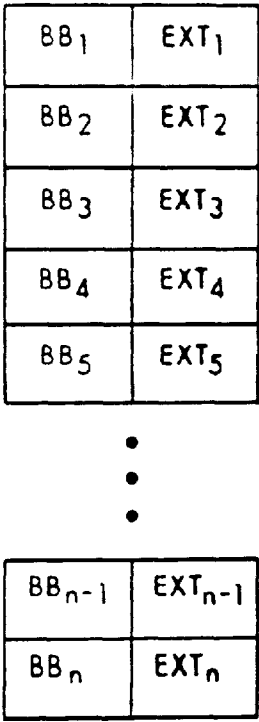
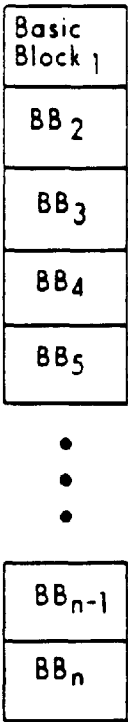
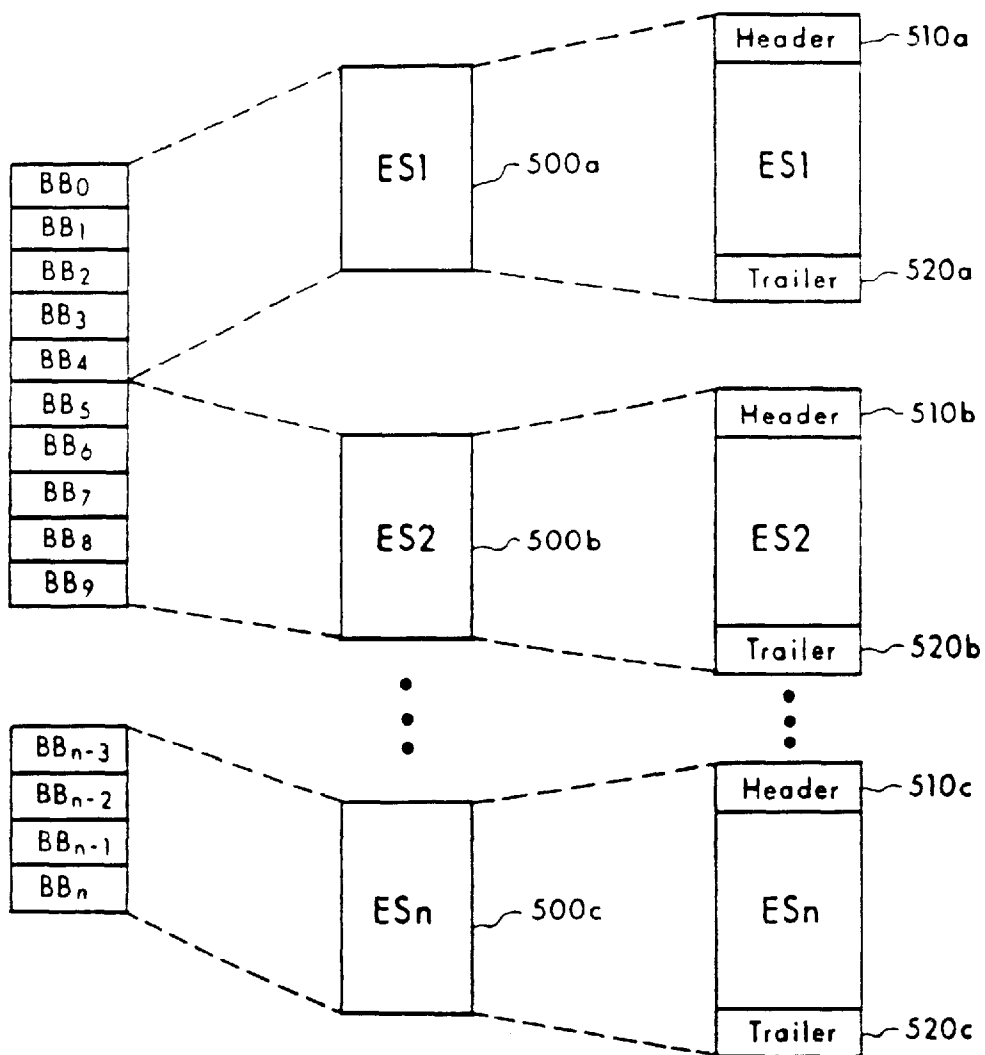


FIG. 3.

FIG. 4

IO	LPN ₀	IFT ₀	SCSM ₀
I1	LPN ₁	IFT ₁	SCSM ₁
⋮			
I _n	LPN _n	IFT _n	SCSM _n

FIG. 5



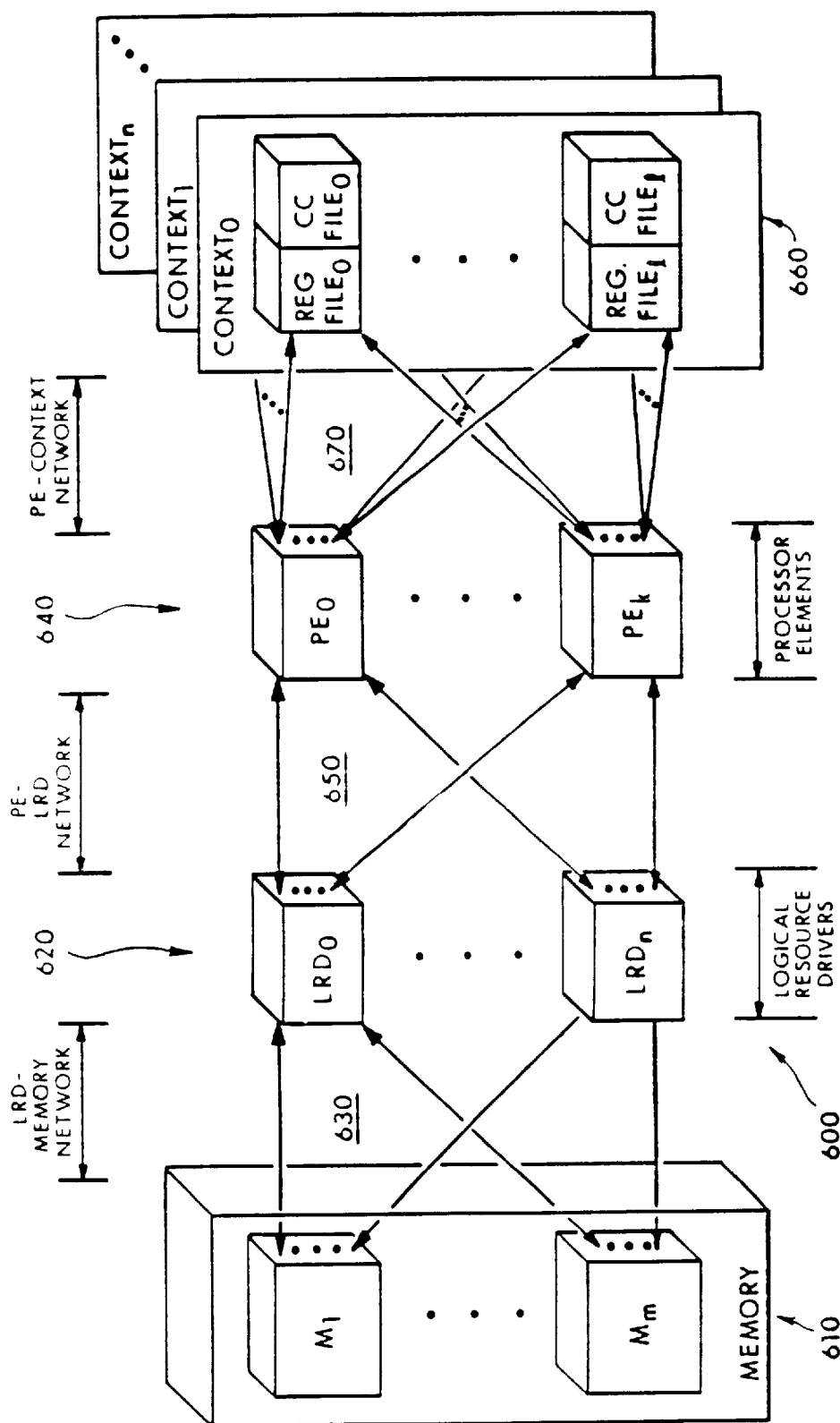
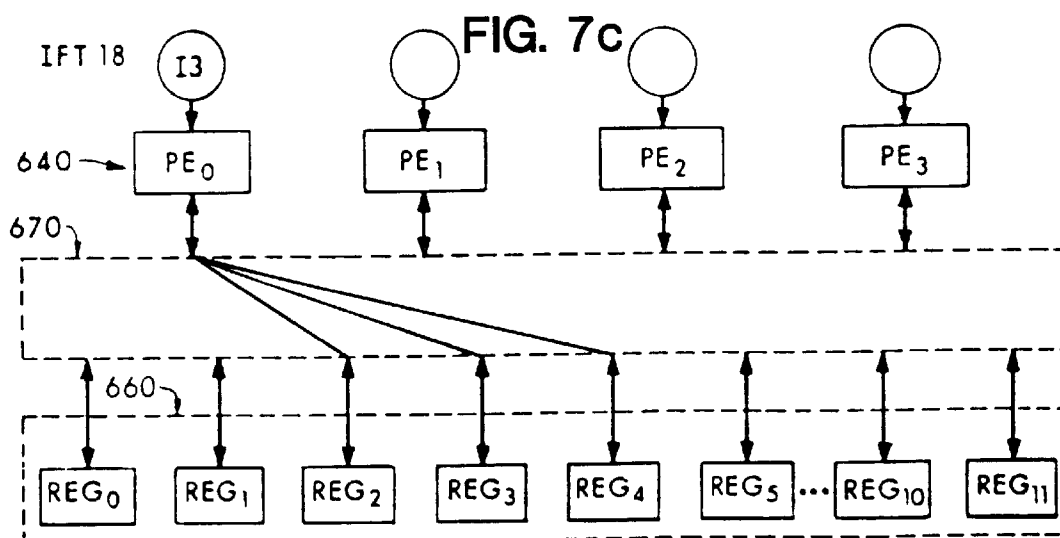
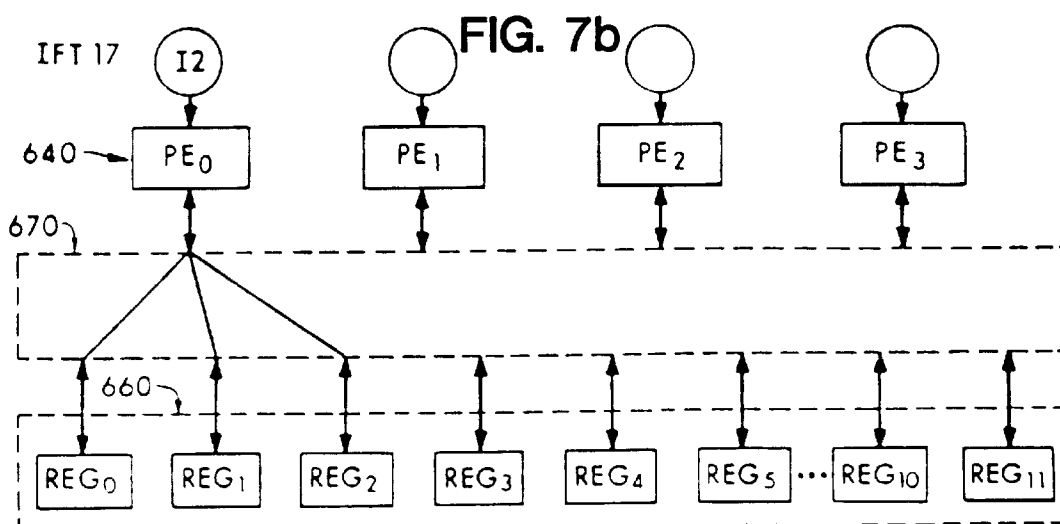
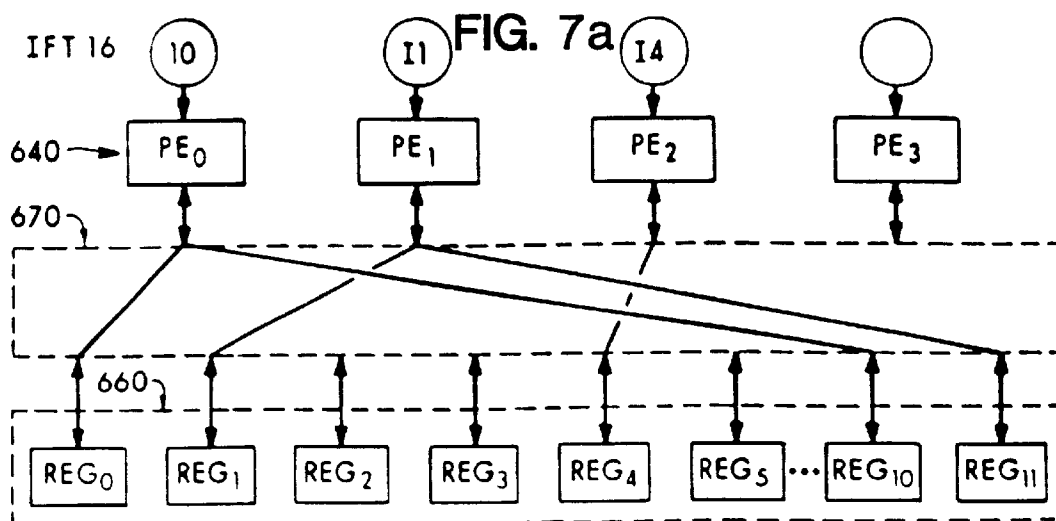
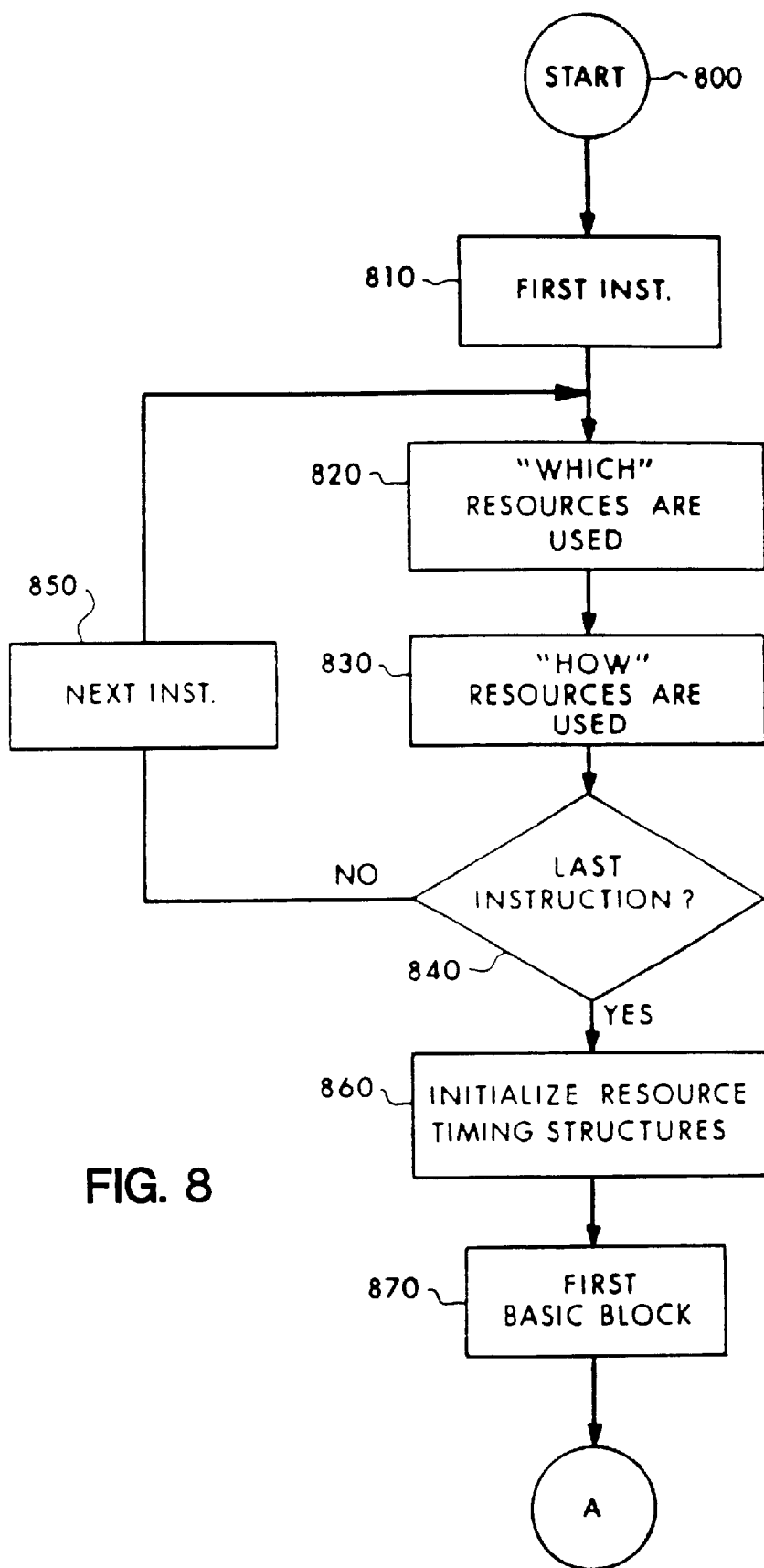


FIG. 6





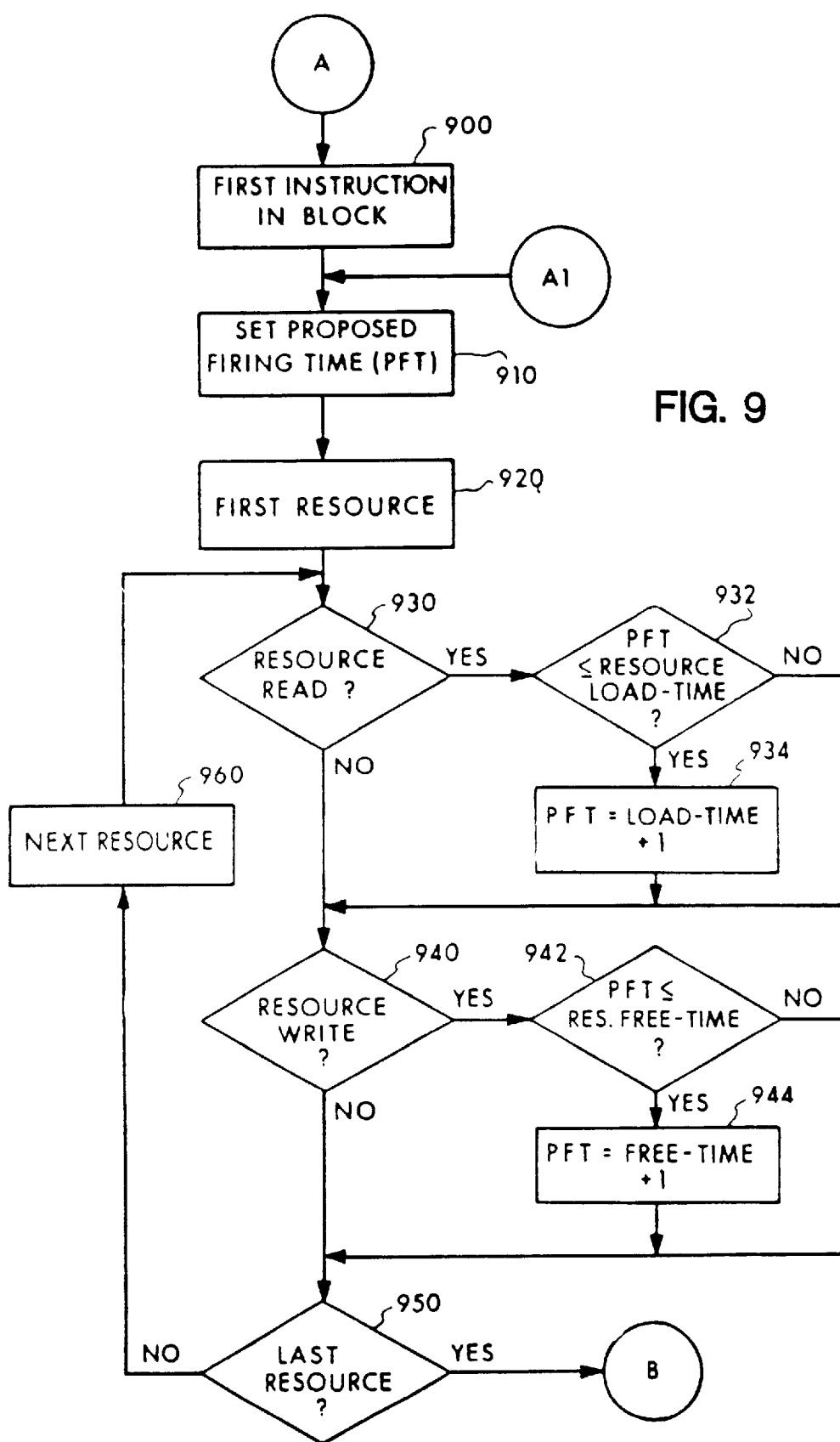
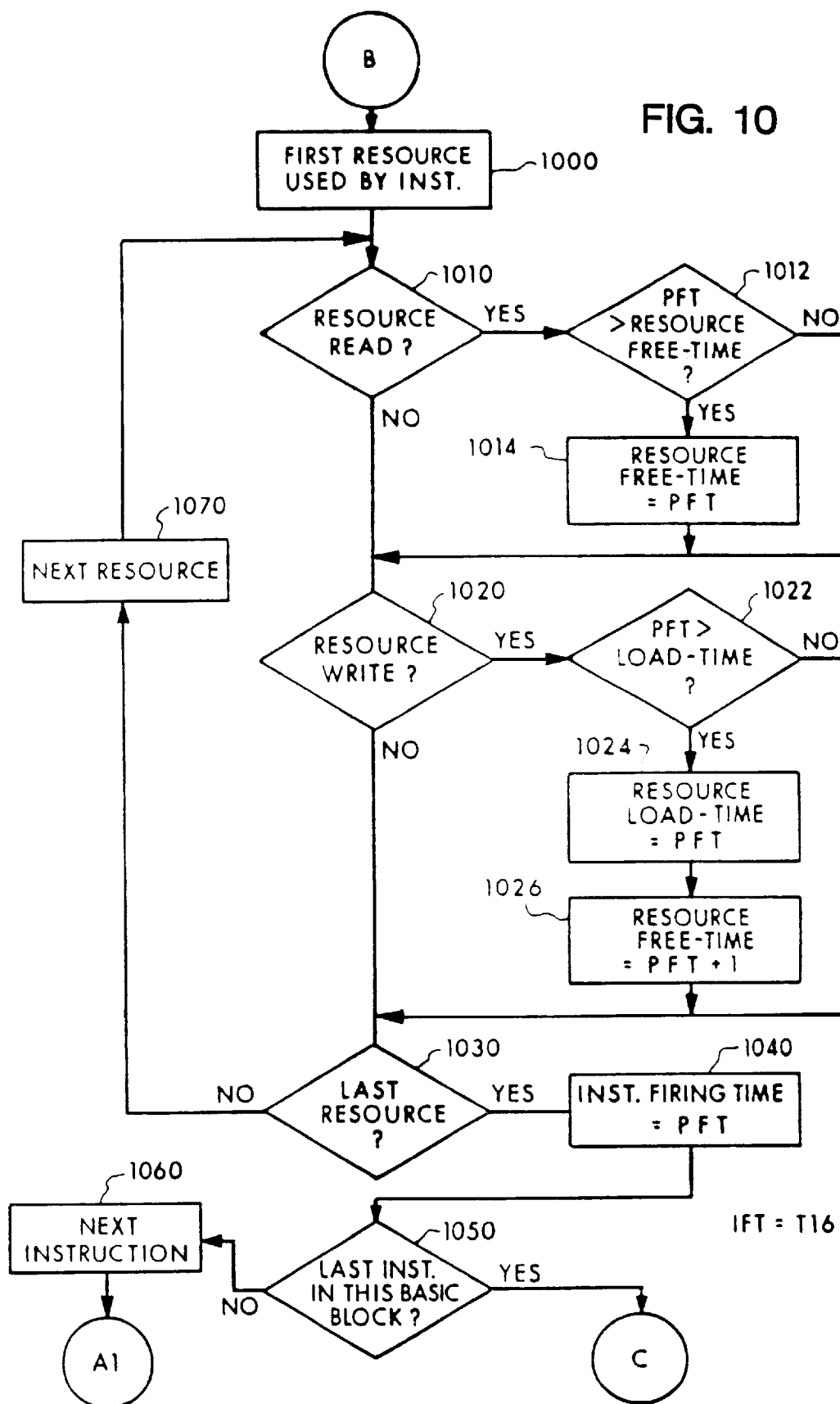
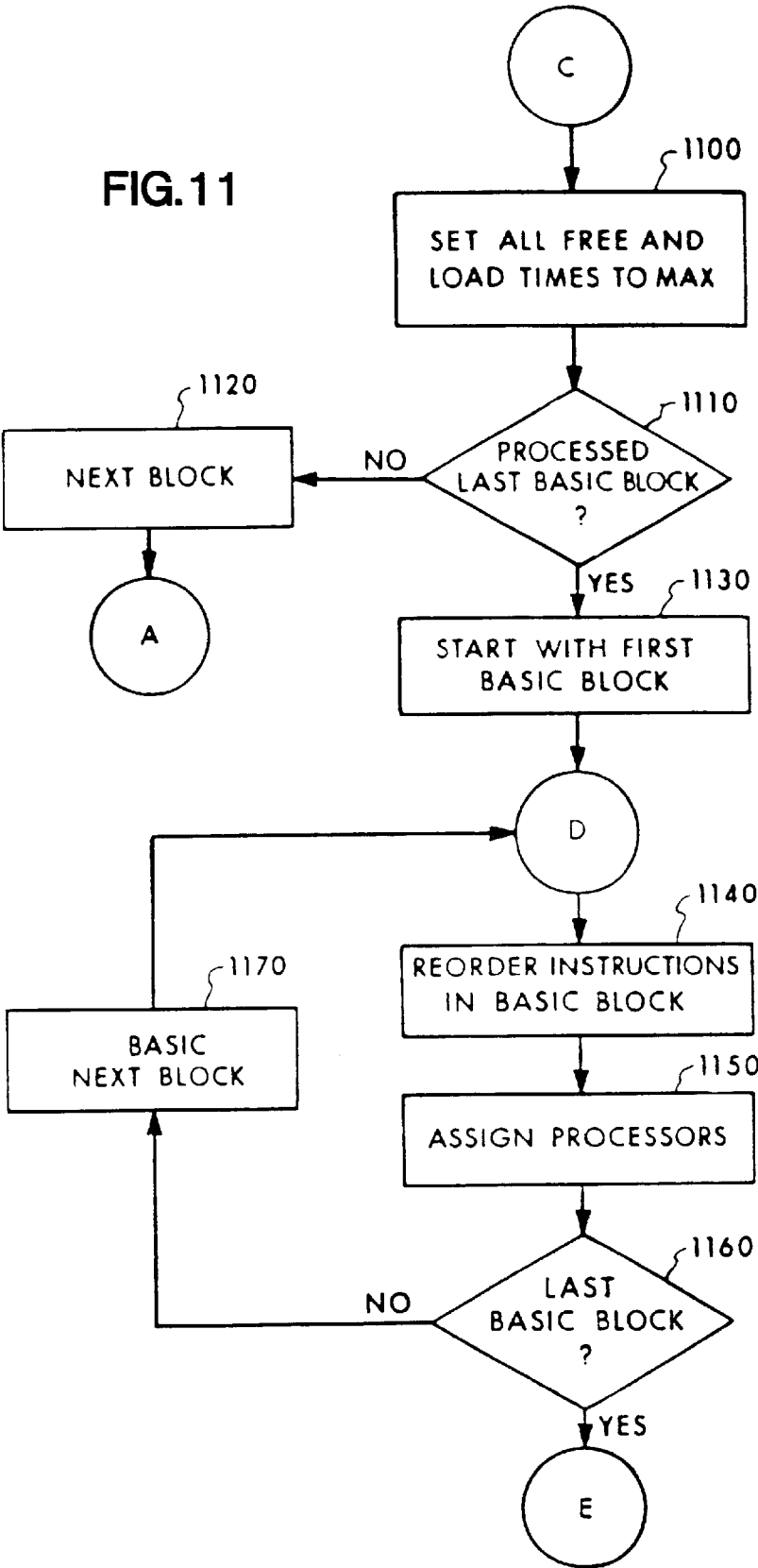


FIG. 10





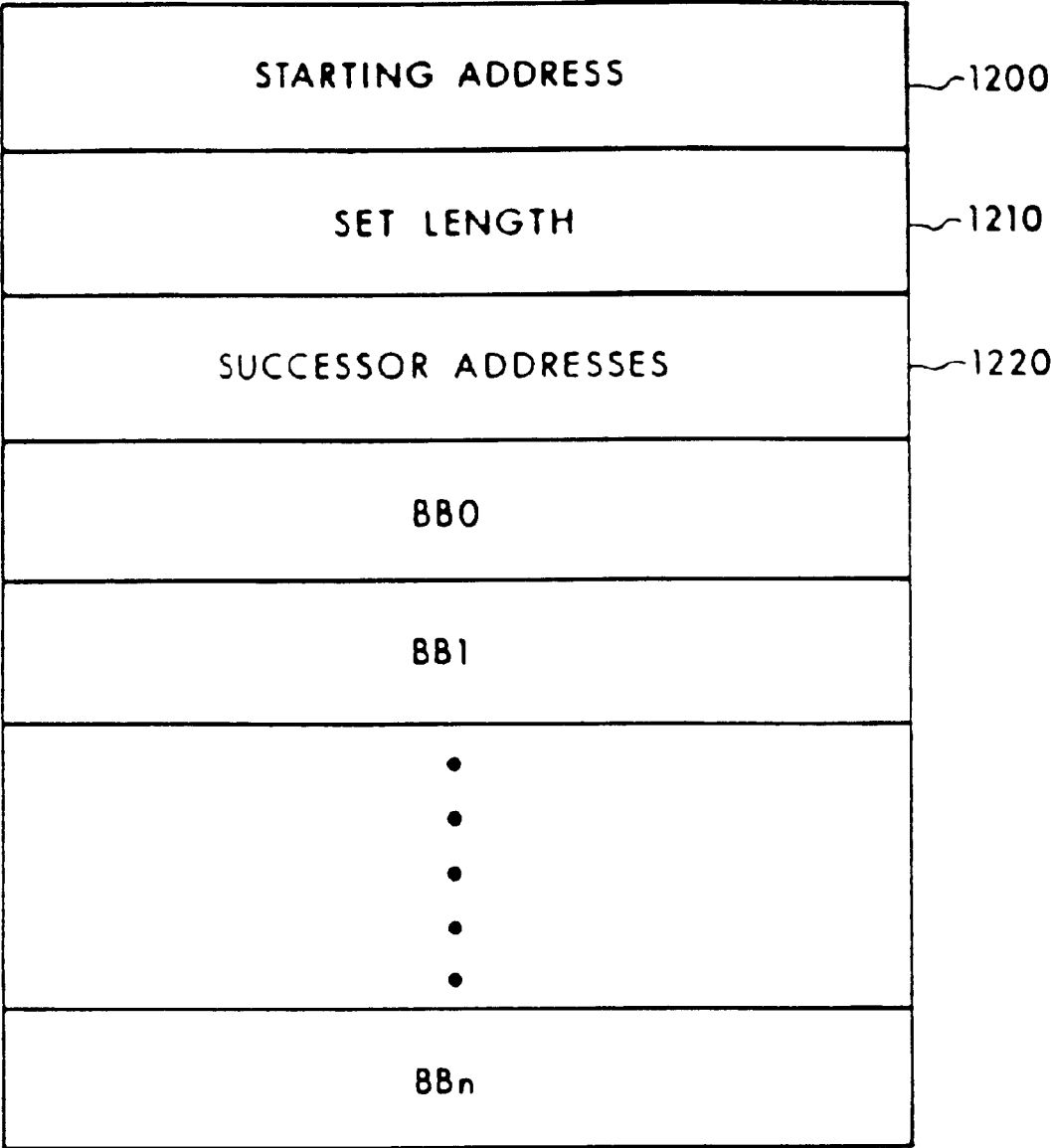


FIG. 12

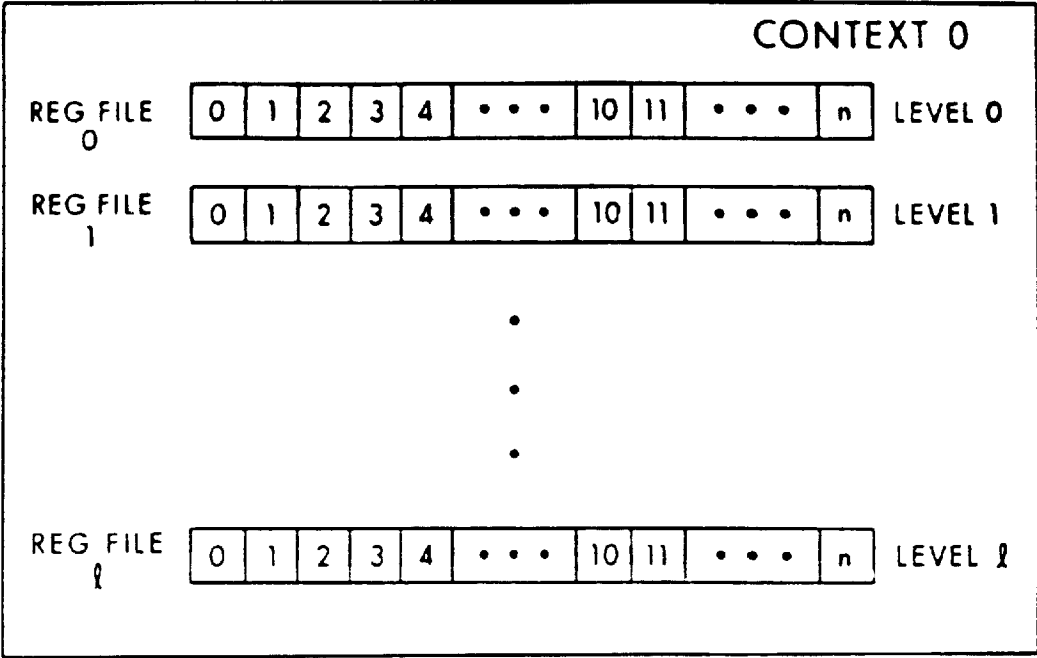


FIG. 13

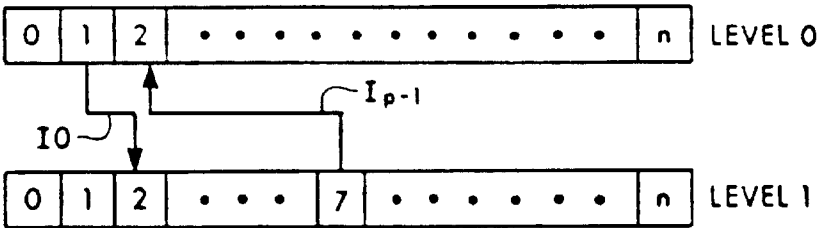


FIG. 14

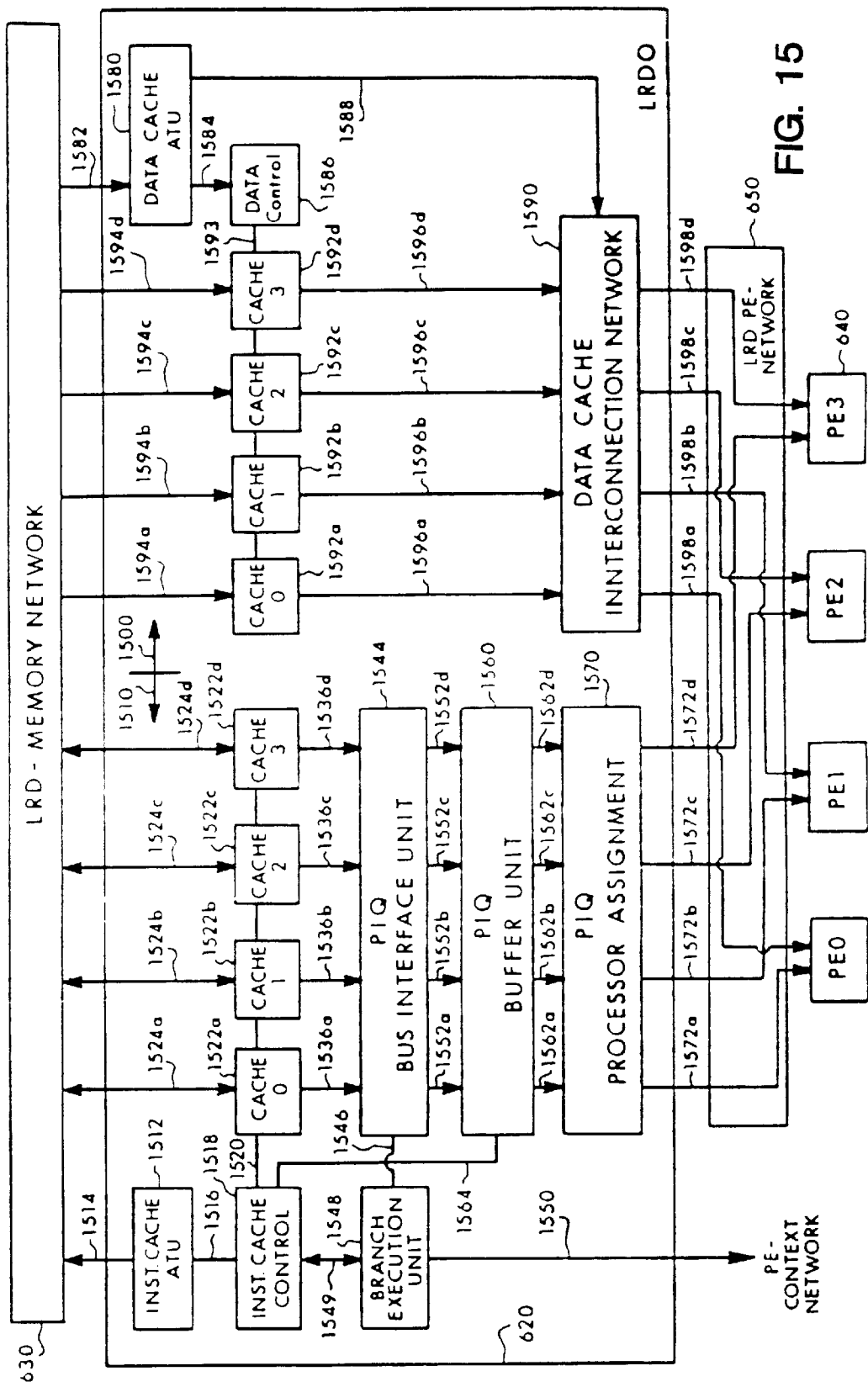


FIG. 15

